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REMARKS

The Office Action of 02/02/2007 has been carefully considered. Reconsideration in view of the foregoing amendments and the present remarks is respectfully requested.

The addition of headings to the specification was suggested. As such headings are not required and have in the past been known to affect the scope of protection afforded, Applicant respectfully declines.

Claims 1-10 were rejected as being unpatentable over Ishida in view of Tomita. The claims have been amended to more clearly distinguish over the cited references. Reconsideration is respectfully requested.

In particular, the claims have been amended to make clear that drive strengths required to write data into individual ones of the memory cells, relative to a drive strength of the bit line circuits, are reduced *in dependence upon a number of memory cells being simultaneously written*, at least during simultaneous writing of data into the memory cells in a plurality of the rows.

In Ishida, by contrast, any reduction in drive strengths required to write data because of internal voltage decreasing circuit 11 is believed to apply under all conditions. That is, there is no dependence of the reduction of drive strength on the number of memory cells being simultaneously written, as presently claimed.

Withdrawal of the rejections and allowance of claims 1-10 is respectfully requested.

Respectfully submitted,

A handwritten signature in dark ink, appearing to read "M. Ure", is written over a horizontal line.

Michael J. Ure, Reg. 33,089

Dated: 07/02/2007